

SELF-CALIBRATION METHOD AND SYSTEM FOR SYNTHESIZERS

By

DENNIS J. HRNCIRIK

AND

BRIAN E. KLOSTERMAN

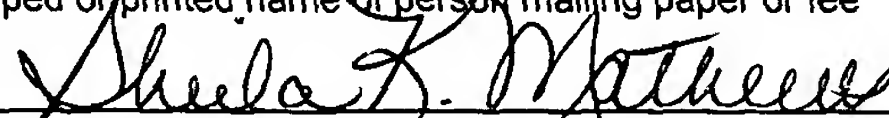
Express Mail Mailing Label EV 228571119 US

Date of Deposit September 11, 2003

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. §1.10 on the date indicated above and is addressed to the Commissioner of Patents, Mail Stop Patent Application, Alexandria, VA 22313-1450.

Sheila K. Mathews

Typed or printed name of person mailing paper or fee


(Signature of person mailing paper or fee)

FIELD OF THE INVENTION

The present invention generally relates to electronics, and more particularly relates to synthesizer phase lock loop circuits, and even more particularly relates to methods and systems for self-calibration of such circuits.

BACKGROUND OF THE INVENTION

In the past, synthesizers with phase lock loops (PLLs) which operate over a wide frequency range typically must adjust loop gain in order to maintain the desired bandwidth (BW). It has been well known that $PLL\ BW = M \times K_p \times K_v / N$ where M is the integrator gain, K_p is phase detector gain, K_v is the voltage controlled oscillator (VCO) tune sensitivity, and N is the loop division ratio.

A prior art synthesizer is shown in Figure 1. Typically, such synthesizers require that the VCO K_v be measured across the entire frequency band. Typically, this K_v measurement requires the synthesizer to be connected to external test equipment. From the K_v measurement, the optimum M or K_p can be determined to achieve the desired BW. Typically, the M or K_p is set either from an external control device or saved in a programmable memory within the synthesizer circuit. In such circuits, expensive VCOs with very tight K_v tolerances are used to minimize variability and shorten the test measurement time. If such synthesizers need repair, it is essential that a similar VCO with the same tight tolerances be used in the repaired device. If modifications are made to the circuit, it often is necessary to recalibrate (readjust M or K_p) the circuit. This requires time and expense.

Consequently, there exists a need for improved methods and systems for calibration of a synthesizer phase lock loop and automate the calibration process.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a synthesizer phase lock loop with enhanced abilities for efficient calibration.

It is a feature of the present invention to utilize a self-calibration scheme.

It is another feature to provide a method to determine the VCO sensitivity without the use of external test equipment.

It is another feature to provide a microcontroller to determine the appropriate adjustment needed in the PLL gain to achieve a desired BW.

It is another feature to provide a microcontroller to set the PLL gain by controlling the phase detector gain, integrator value, or some other gain determining circuit to achieve the desired BW.

It is an advantage of the present invention to provide for individual self-calibration of a synthesizer PLL.

The present invention is a system and method for self-calibration of a synthesizer PLL which is designed to satisfy the aforementioned needs, provide the previously stated objects, include the above-listed features and achieve the already articulated advantages. The present invention is carried out in a manner that the need to predetermine a VCO's sensitivity across the operating range has

been eliminated, or at least has been greatly reduced, which reduces the cost of test setup and eliminates the expense imposed by a requirement for VCOs with very tight tolerances.

Accordingly, the present invention is a synthesizer PLL with a microcontroller with an analog-to-digital converter to automatically measure, compute, select and store the appropriate gain to achieve the desired PLL BW.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may be more fully understood by reading the following description of the preferred embodiments of the invention, in conjunction with the appended drawings wherein:

Figure 1 is a block diagram of a prior art PLL disposed within the dotted line.

Figure 2 is a block diagram of a PLL of the present invention disposed within the dotted line.

DETAILED DESCRIPTION

Now referring to the drawings wherein like numerals refer to like matter throughout, there is shown a synthesizer PLL and control system of the prior art, generally designated 100, which includes PLL circuit 102, having a voltage controlled oscillator (VCO) 104. VCO 104 has a tune sensitivity of K_v . PLL 102 includes an integrator 106, with an integrator op-amp 108, an integrator resistor 110, and an integrator capacitor 112. The gain of integrator 106 is represented by the variable M . The effective resistance of input resistor 116 disposed between the phase detector 132 and the integrator op-amp 108, is controlled by the MUX 114. MUX 114 is controlled by the EEROM 120 which stores in a non-volatile manner, the optimum resistance (or M) setting in a look-up table. The gain of phase detector 132 is represented by K_p and may also be varied and controlled to adjust the PLL gain. A frequency reference 130 provides a signal to phase detector 132. Divider 134 is labeled with variable N , which is the loop division ratio. Changes in N affect the RF output frequency of VCO 104.

Typically during production of a prior art PLL 102, the equation $PLL\ BW = M \times K_p \times K_v / N$, is used to compute the appropriate M and K_p to optimize the BW at any given frequency within the operating range of the PLL 102. For example, a frequency data signal 122 is supplied to EEROM 120 and divider 134. A test connector 124 and test connector 126 are used to monitor the tune voltage into VCO 104 and control the variable resistance at MUX 114 at various frequencies. Based upon the measurements over the entire operating range, the EEROM 120

is loaded with the appropriate data which is used during normal operation of the PLL to set the PLL BW at the various frequencies.

Now referring to Figure 2, there is shown a PLL and control circuit system of the present invention, generally designated 200. A PLL 202, which is very similar to the prior art PLL 102, except that it includes a microcontroller 220 which provides data and control, receives feedback of the tune voltage. Microcontroller 220 can be any suitable type of microcontroller. This microcontroller may take the place of field programmable gate arrays (FPGAs), which are often used in prior art synthesizers to perform other tasks, such as convert system frequency commands to more synthesizer-friendly serial or parallel code, band selection, hop control, etc. The VCO 204 may be identical to VCO 104 except that it may be permissible to utilize less expensive VCOs with less tight tolerances, owing to the ability to self-calibrate. System 200 also includes a digital potentiometer (pot) 240 which receives a modulation signal from modulation source 250. The digital pot provides a means to control the modulation signal to integrator op-amp 108.

In operation, the system and method of the present invention could function as follows:

The PLL is implemented in a circuit or IC. The microcontroller 220 provides control signals to divider 134, digital pot 240, phase detector 132 and MUX 114; the BW is maximized by manipulation of these control signals as is

determined by a feedback of the tune voltage using the above-described formula for optimized bandwidth. This self-calibration can be done at various times. Self-calibration can be limited to once at initial power-up at a factory test. It can be done on every power-up and then be saved in either volatile or non-volatile memory. For fixed or relatively slow tune synthesizer applications, the self-calibration can be done every time the frequency is changed and/or powered up.

In view of the high level of skill in the art known by designers of prior art synthesizer PLLs, it is thought that the method and apparatus of the present invention will be understood from the foregoing description, and that it will be apparent that various changes may be made in the form, construct steps and arrangement of the parts and steps thereof, without departing from the spirit and scope of the invention or sacrificing all of their material advantages. The form herein described is merely a preferred exemplary embodiment thereof.